UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/700,391	11/04/2003	Arun Radhakrishnan	5500-91300	5786

53806 7590 04/06/2007
MEYERTONS, HOOD, KIVLIN, KOWERT & GOETZEL (AMD)
P.O. BOX 398
AUSTIN, TX 78767-0398

EXAMINER	
JOHNSON, BRIAN P	
ART UNIT	PAPER NUMBER
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No. 10/700,391	Applicant(s) RADHAKRISHNAN ET AL.	
	Examiner Brian P. Johnson	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 28 December 2006.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) 1-24 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-24 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-24 are pending.

Papers Filed

2. Examiner acknowledges receipt of a request for continued examination on 24 July 2006.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-8, and 11-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Pontius et al. (U.S. Patent No. 6,029,243) hereinafter referred to as Pontius.

5. As per claim 1, Pontius discloses a processor comprising:

a prediction circuit configured to predict an execution latency of a floating point operation responsive to a predicted precision of the floating point operations; (Col. 2 line 65 – col. 3 line 18) *The examiner asserts that Pontius inherently predicts execution latency based on the requested result (predicted precision). When an extended-precision operation is requested, the execution unit cannot perform the higher-precision*

function, and the operation is predicted to take a long time as a trap must be called and a software multiply must occur. As disclosed in col. 3 lines 4-18, if the operands are of sufficiently small precision, the operation will execute more quickly than expected.

A scheduler configured to schedule a floating point operation for execution (col 4 lines 3-20),

Note that the LAD and LAE modules gather information used to determine how (and by which mechanism) the floating point instruction will be executed. The "scheduler" is considered to be the control device that uses this information to control the functionality disclosed in col 2 line 65 to col 3 line 18).

wherein the prediction circuit is configured to predict the execution latency prior to the floating point operation being scheduled by the scheduler for execution (col. 2 line 65 to col 3 line 18);

Note that, clearly, the prediction must be made prior to the scheduling for the processor to determine if the instruction is to be scheduled to the execution unit or the software trap.

and a floating point unit (Fig. 1 Execution Unit EXU in combination with Trap Logic TPL) coupled to receive the floating point operation for execution scheduled by the scheduler, wherein the floating point unit is configured to detect a misprediction of the execution latency. (Col. 4 lines 3-20 and lines 45-48)

6. As per claim 2, Pontius discloses a processor as recited in claim 1 wherein the predicted precision is a precision of the floating point operation. (Col. 2 lines 25-35)

7. As per claim 3, Pontius discloses the processor as recited in claim 2 wherein the floating point unit comprises a control register storing a precision control indication indicative of an output precision for the floating point operation, wherein the predicted precision is the output precision. *Lines PH and PL indicate the desired precision of the floating point operation. The values are translated to D/S signal by the trap logic.*

8. As per claim 4, Pontius discloses the processor as recited in claim 2 wherein the floating point operation is a multiply operation (Col. 1 line 13), and wherein the floating point unit comprises a multiplier designed for a first precision less than a maximum precision supported by the processor, (Col. 2 line 65 – col. 3 line 18) and wherein the execution latency is based on a number of passes through the multiplier used to complete a multiplication of the precision of the operands. *The examiner asserts that there is a higher latency when the operation passes through the multiply circuitry zero times (when it is performed by software) and has a lower execution latency when it passes through once.*

9. As per claim 5, Pontius discloses the processor as recited in claim 2 wherein the floating point unit comprises a precision check circuit coupled to receive the operands of the floating point operation, wherein the precision check circuit is configured to detect the misprediction if at least one of the operands of the floating point operation has a precision that exceeds the predicted precision. (Col. 4 lines 3-20)

10. As per claim 6, Pontius discloses the processor as recited in claim 1 wherein the floating point unit is configured to signal the scheduler responsive to detecting the misprediction. *The examiner asserts that Pontius' processor inherently contains a scheduler, as instructions are scheduled to operate on the processing logic. Further, the scheduler must inherently be alerted to the mispredicition (col. 4 lines 45-48) as it must temporarily hold any subsequent instructions which have data dependencies to the result of the mispredicted one. If it were to issue the second instruction before the first finished, improper results may be obtained.*

11. As per claim 7, Pontius discloses the processor as recited in claim 6 wherein the scheduler is configured to reschedule the floating point operation responsive to the signaling from the floating point unit with the execution latency indicated as a latency detected by the floating point unit. *The examiner asserts that the second operation (which was temporarily held) may be issued once the data dependency has been resolved.*

12. As per claim 8, Pontius discloses the processor as recited in claim 6 wherein the prediction circuit is configured to predict the execution latency of the floating point operation responsive to dispatch of the floating point operation to the scheduler. *The examiner asserts that the execution latency can be measured from any point in the processing pipeline, including upon issuance to the scheduler.*

13. As per claim 11, Pontius discloses the processor as recited in claim 1 wherein the floating point unit is configured to signal an exception responsive to detecting the misprediction. (Col. 4 lines 3-20)

14. As per claim 12, Pontius discloses the processor as recited in claim 11 wherein the processor is configured to refetch the floating point operation responsive to the exception. *The examiner asserts that issuing the instruction to the "Extended-Precision Floating-Point Subroutines" SUB constitutes a refetch.*

15. As per claim 13, Pontius discloses the processor as recited in claim 1 wherein the floating point unit is configured to detect the misprediction responsive to detecting an actual execution latency greater than the execution latency predicted by the prediction circuit. *The examiner asserts that the execution unit detects the misprediction described in col. 4 lines 45-48. Since the instruction must be completed by the SUB block of Fig. 1, and the operation of the SUB block is known to have a higher execution latency than the operation performed by the execution unit, the higher execution time is inherently detected.*

16. As per claim 14, Pontius discloses the processor as recited in claim 13 wherein the floating point unit is configured not to detect the misprediction responsive to detecting the actual execution latency is less than the execution latency predicted by

the prediction circuit. *Pontius discloses adding logic to a first embodiment to enable detection of the case where an operation has been requested (predicted) to be performed as an extended-precision operation but the precision of the operands is sufficiently small to enable processing in hardware (col. 3 lines 4-18). Pontius' first embodiment does not detect the misprediction, but rather sends the sufficiently-small operands to the software block to be processed.*

17. As per claim 15, Pontius discloses the processor as recited in claim 13 wherein the floating point unit is further configured to detect the misprediction responsive to detecting the actual execution latency is less than the execution latency predicted by the prediction circuit. *Pontius discloses adding logic to a first embodiment to enable detection of the case where an operation has been requested (predicted) to be performed as an extended-precision operation but the precision of the operands is sufficiently small to enable processing in hardware (col. 3 lines 4-18).*

18. Claim 16 is directed toward a method performing the functions of the processor of claim 1 and is rejected under the same grounds.

19. Claim 17 is directed toward a method performing the functions of the processor of claim 2 and is rejected under the same grounds.

20. Claim 18 is directed toward a method performing the functions of the processor of claim 4 and is rejected under the same grounds.

21. Claim 19 is directed toward a method performing the functions of the processor of claim 5 and is rejected under the same grounds.

22. Claim 20 is directed toward a method performing the functions of the processor of claim 7 and is rejected under the same grounds.

23. Claim 21 is directed toward a method performing the functions of the processor of claims 11 and 12 and is rejected under the same grounds.

24. Claim 22 is directed toward a method performing the functions of the processor of claim 13 and is rejected under the same grounds.

25. Claim 23 is directed toward a method performing the functions of the processor of claim 14 and is rejected under the same grounds.

26. Claim 24 is directed toward a method performing the functions of the processor of claim 15 and is rejected under the same grounds.

Claim Rejections - 35 USC § 103

27. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

28. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pontius.

29. As per claim 9, Pontius discloses the processor as recited in claim 6 but fails to disclose it further comprising a trace cache configured to store predicted operation traces, wherein the prediction circuit is configured to predict the execution latency responsive to the floating point operation being included in a trace, and wherein the trace cache is configured to store an indication of the execution latency predicted by the prediction circuit.

30. Official notice is taken that trace caches are extremely well known in the art.

31. Trace caches store commonly used strings (or traces) of operations in order of execution for the benefit of more easily recalling said traces for subsequent execution. This benefit is in line with a desired outcome of Pontius' invention of decreasing execution latency and increasing instruction throughput.

32. It would have been obvious to one of ordinary skill in the art at the time of invention to have included a trace cache in Pontius' invention for the benefit of instruction throughput.

33. As per claim 10, Pontius discloses the processor as recited in claim 9 wherein the trace cache is configured to store a selected opcode of at least two opcodes for the floating point operation responsive to the execution latency predicted by the prediction circuit, the selected opcode comprising the indication of the execution latency. *The examiner asserts that if an instruction is to be issued from a trace cache, it must inherently contain an indication of the operation to be performed. This indication (opcode) must include the PH and PL signals, as Pontius' processor will not function properly without those signals. Further, these signals may indicate one of up to three opcodes – a single precision, double precision or extended precision operation.*

Response to Arguments

Applicant's arguments filed 28 December 2007 have been fully considered but they are not persuasive.

1. Applicant states:

"Claim 1 recites a combination of features including: 'a scheduler configured to schedule the floating point operation for execution wherein the prediction circuit is configured to predict the execution latency prior to the floating point operation being scheduled by the scheduler for execution.". . . A trap is normally signaled in a processor during the execution of the instruction." There is no need to know, prior to scheduling the instruction for execution, whether or not the instruction will trap."

Examiner is no concerned about how traps are "normally" signaled, but rather how the operation of Pontius is executed. Fig. 1 of Pontius clearly shows that the trap logic predicts the mechanism for execution outside of the execution unit, and outputs the results to the SUB and EXU.

Perhaps even clearer is fig. 2, which shows that a prediction is made in S2 and, based on the result, the instruction is scheduled to either hardware execution (S3) or a trap (S4).

2. Applicant states:

"Additionally, the Office Action asserts that the scheduler recited in claim 1 is the control device that uses the LAD and LAE information to determine the mechanism for execution the floating point instruction. However, the trap logic TPL detects the trap based on the operands read from the register bank. The operands read from the register bank are also provided directly to the execution unit EXU for execution (see Fig. 1, INA and INB). Thus, it is very clear that the operation of the TPL unit to detect the trap on the LAE occurs after the instruction is scheduled for the execution. This contradicts the assertion in the Office Action, since the scheduler must schedule the instruction for execution without the LAE/LAD information."

In the first sentence above, Applicant has correctly quoted Examiner's interpretation of the scheduler. Applicant then states that because some instruction information is routed directly to the execution unit, then it must follow that the operation of the TPL to detect the trap on the LAE occurs after the instruction is scheduled for

execution. This conclusion is drawn just three sentences later and already Applicant abandoned Examiner's interpretation.

By definition, it is impossible for a scheduler that "uses the LAD and LAE information to determine the mechanism for execution of the floating point instruction" to also "schedule the instruction for execution without the LAE/LAD information." Examiner reiterates; the TPL logic of fig. 1 predicts the execution latency. This step is represented by S2 if fig. 2. Fig. 2 makes it overtly obvious that the outcome of this prediction is required to schedule the instruction to either the Hardware Execution (S3) or the Trap (S4). This scheduling must be done after the prediction, because the prediction information is required to do the scheduling.

Applicant has chosen, apparently, to take the mechanism that sends operand data to the execution unit and call that a "scheduler". This is not Examiner's interpretation. The fact that operand information is sent to the execution so it is ready in case the instruction is executed there does not change Examiner's interpretation.

3. Applicant states:

"Still further, the Office Action asserts that the TPL is part of the floating point execution unit (see Office Action, page 3, fifth full paragraph). Again, this contradicts the above assertion."

Examiner recognizes this confusion and understands that some explanation is required. Examiner's note that the floating-point unit includes the EXU in combination with the TPL logic was made in anticipation of claim 3. It was not Examiner's intention

for the interpretation of the "Floating Point Unit" to encompass all of the TPL logic, but rather a portion. In particular, with regard to fig. 3, the floating-point unit is interpreted to include the control register with the PH and PL information, as required by claim 3. Examiner's statement has been removed to rectify this ambiguity.

4. Applicant states:

"Still further, the Office Action asserts that Pointius inherently predicts the execution latency based on the requested result precision (See Office Action, page 2, last paragraph extending to page 3). Applicants respectfully disagree. The requested result precision, along with the operand bits, are used by the LAE and LAD in the TPL to detect a hardware-unsupported precision to signal a trap. No prediction is made...rather the op is decoded and the requested precision is provided at execution time. For example, Pontius teaches: "Logic for selecting execution precision is used to determine whether an operation is to be performed in hardware or in software (in response to a trap). A simple approach is to set the execution precision equal to the maximum of the requested result precision and the maximum apparent precision of the operands. When the execution precision is within the capability of the execution unit, the operation is performed in hardware; when the execution precision is too high for the execution unit, a trap is executed to initiate execution in software. In this approach, a high requested result precision always results in a trap." (Pontius, col. 2, line 50-col. 3, line 3). The discussion is part of the summary, and is effectively discussing the operation of the LAE and the LAD in the TPL. Clearly, the above discussion refers to

using the requested precision at execution time to determine if a trap is signaled or not. There is no teaching or suggestion that the requested precision is used at any other time to make any sort of prediction."

Examiner disagrees. Applicant gives a theoretically accurate description of the invention of Pontius, but does not believe that such functionality includes a prediction. It appears that Applicant desires an indication of a misprediction. This is shown in col. 4 lines 44-48.

"As noted in the Response to Final Office Action with regard to claim 8, merely measuring the latency from any desired point in the pipeline does not teach or suggest the 'prediction circuit is considered to PREDICT the execution latency of the floating point operation responsive to dispatch of the floating point operation to the scheduler". The Advisory Action asserts that the LAE and LAD hardware is used to make the prediction, and the information is utilized to schedule the instruction. However, as pointed about [sic: out?] above, the LAE and LAD hardware operate at execution time to determine the precision. The assertion that the LAE and LAD hardware are considered to be a scheduler, as alleged in the Advisory Action, conflicts with the Office Action's assertion that the TPL (which includes the LAE and LAD hardware) is part of the floating point execution unit."

This appears to be a reiteration of other arguments, which are addressed above.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P. Johnson whose telephone number is (571) 272-2678. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Eddie Chan

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100